



The 21st IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'06)

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Hilton Arlington & Towers, Arlington/Washington DC, USA



Sponsored by the IEEE Computer Society, Fault-Tolerant Computing Technical Committee, and Test Technology Technical Council

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Call for Papers

DFT'06 will be held in Arlington/Washington DC, USA, at the Hilton Arlington & Towers Hotel. The hotel is located in the upscale Ballston area of Arlington, Virginia and is linked by skybridge to the Ballston Common Mall and NSF Office Complex. The Ballston neighborhood provides close proximity to high-tech engineering firms and government research offices.

This symposium provides an open forum for presentations in the field of defect and fault tolerance in VLSI systems inclusive of emerging technologies. One of the unique features of this symposium is to combine new academic research with state-of-the-art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. The topics include (but are not limited to) the following ones:

- 1. Yield Analysis, Modeling and Enhancement**
Defect/Fault analysis and models; statistical yield modeling; critical area and other metrics.
- 2. Repair, Restructuring and Reconfiguration**
Repairable logic, fault-isolation, reconfiguration, and repair; restructurable and reconfigurable circuit design; on-line reconfiguration and repair.
- 3. Testing Techniques**
Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits.
- 4. Error Detection, Correction, and Recovery**
Self-testing and self-checking design; error-control coding; fault masking logic design; recovery scheme using space/time redundancy.
- 5. Defect and Fault Tolerance**
Reliable circuit synthesis; radiation hardened/tolerant processes and design; transient/soft faults (SEU) tolerance, delay defect/fault tolerance.
- 6. Dependability Analysis and Validation**
Fault injection techniques and environments; dependability characterization of IC and systems.
- 7. Emerging Technologies**
Defect and fault tolerance in Carbon Nanotubes, Quantum-dot Cellular Automata, Quantum Computing, and Single Electron Transistors.
- 8. Safety Critical Systems**
Design for defect and fault tolerance in safety critical systems and applications such as: automotive, railway, avionics, industrial control, and space.

Prospective authors should prepare an extended summary or the full paper (up to 9 pages in the IEEE 6X9 format), to be submitted as PDF file. Uncompressed unencapsulated postscript may also be used when necessary. Submission will be electronically only. Use the contact author's last name as file name; add numerals in the case of multiple submissions (e.g., lo1, lo2). Detailed information about the submission process will be made available on the symposium web page:

<http://netgroup.uniroma2.it/DFT06/>

Authors should notify their submission to the Program Chairs by e-mail, indicating the title, authors' names, affiliation, mail address, phone, fax and e-mail and the name of the contact author. The submission should also indicate the intended presenter. We are also interested in panel sessions that involve industrial experiences: please send an email to the Program Chairs with a brief description (1 page maximum) of the panel discussion you would like to propose.

Prospective authors should adhere to the following deadlines:

Submission deadline:	May 31, 2006
Notification of acceptance:	June 30, 2006
Camera ready full papers:	July 31, 2006

The proceedings will be published by the IEEE Computer Society. Authors will have the opportunity to submit extended versions of the papers published at the symposium in a special issue of a journal.

For general information, contact the General co-Chairs. For paper submission information, contact the Program co-Chairs. For all updated information concerning the symposium, visit our Web page.