THE 21ST IEEE INTERNATIONAL SYMPOSIUM ON DEFECT AND FAULT TOLERANCE IN VLSI SYSTEMS

Preliminary Program Schedule

Wednesday, October 4

7:50am - 8:20am Registration

8:20am - 9:30am

- **Welcoming Remarks**
- **Invited Talk:**
  SINGLE-EVENT-UPSET TRENDS IN ADVANCED CMOS TECHNOLOGIES
  David HEIDEL
- **Invited Talk:**
  Sankar Basu, National Science Foundation

9:50am - 11:10am Session 1: Adaptive Design and Gate Level Redundancy

1. **ADAPTIVE DESIGN FOR PERFORMANCE-OPTIMIZED ROBUSTNESS**
   RAMYANSHU DATTA, Jacob ABRAHAM, Abdulkadir UTKUDIRIL, Abhijit CHATTERJEE, Kevin NOWKA
2. **EMPLOYING ON-CHIP JITTER TEST CIRCUIT FOR PHASE LOCKED LOOP SELF-CALIBRATION**
   Tian XIA, Stephen WYATT, Rupert HO
3. **IMPROVING YIELD AND DEFECT TOLERANCE IN MULTIFUNCTION SUBTHRESHOLD CMOS GATES**
   KRISTIAN GRANHAUG, Snorre AUNET
4. **GATE FAILURES EFFECTIVELY SHAPE MULTIPLEXING**
   Valeriu BEIU, WALID IBRAHIM, Yaser ALI ALKHAWWAR, Mawahib SULIEMAN

11:30am - 12:30pm Session 2: Delay Test

1. **TEST GENERATION FOR OPEN DEFECTS IN CMOS CIRCUITS**
   NARENDRA DEVTA-PRASANNA, Arun GUNDA, Prabhakaran KRISHNAMURTHY, Sudhakar REDDY
2. **IMPLICIT CRITICAL PDF TEST GENERATION WITH MAXIMAL TEST EFFICIENCY**
   Kyriakos CHRISTOU, Maria MICHAEL, Spyros TRAGOUDAS
3. **SELECTING HIGH-QUALITY DELAY TESTS FOR MANUFACTURING TEST AND DEBUG**
   HANGKYU LEE, SURIYAPRAKASH NATARAJAN, Srinivas PATIL, Irith POMERANZ

12:30pm - 1:40pm Lunch

1:40pm - 3:20pm Session 3: Emerging Technologies

1. **TESTING REVERSIBLE 1D ARRAYS OF MOLECULAR QCA**
   XIAOJUN MA, Jing HUANG, Cecilia METRA, Fabrizio LOMBARDI
2. **EFFICIENT AND ROBUST DELAY-INSENSITIVE QCA (QUANTUM-DOT CELLULAR AUTOMATA) DESIGN**
   Minsu CHOI, Myungsu CHOI, Zachary PATITZ, NOHPILL PARK
3. **ERROR TOLERANCE OF DNA SELF-ASSEMBLY BY MONOMER CONCENTRATION CONTROL**
   Yong-Bin KIM, Byunghyun JANG, Fabrizio LOMBARDI
4. **INHERITED REDUNDANCY AND CONFIGURABILITY UTILIZATION FOR REPAIRING NANOWIRE CROSSBARS WITH CLUSTERED DEFECTS**
   Minsu CHOI, Yadunandana YELLAMBALASE, Yong-Bin KIM
5. **A RECONFIGURATION-BASED DEFECT TOLERANCE METHOD FOR NANOSCALE DEVICES**
   Mohammad TEHRANIPOOR, Reza RAD

3:40pm - 5:00pm Session 4: Test Compression

1. **REDUCING ATE BANDWIDTH AND MEMORY REQUIREMENTS: A DIAGNOSIS FRIENDLY SCAN TEST RESPONSE COMPACTOR**
   Sverre WICHLUND, Frank BERNTSEN, EINAR J AAS
2. **A NOVEL METHODOLOGY FOR FUNCTIONAL TEST DATA COMPRESSION BY ATE**
   HAMID REZA HASHEMPUOUR, Fabrizio LOMBARDI
3. **LOW-COST IP CORE TEST USING MULTIPLE-MODE LOADING SCAN CHAIN AND SCAN CHAIN CLUSTERS**
   TOSHINORI TAKABATAKE, Gang ZENG, YOUHUA SHI, Hideo ITO
4. AN EFFICIENT SCAN CHAIN PARTITIONING SCHEME WITH REDUCTION OF TEST DATA UNDER ROUTING CONSTRAINT
   Geewhun SEOK, Il-Soo LEE, Tony AMBLER, Baxter F. WOMACK

7:30pm Reception

Thursday, October 5

8:30am - 9:30am Invited Talk

- **RECONFIGURATION-BASED DEFECT TOLERANCE FOR MICROFLUIDIC BIOCHIPS**
  Krishnendu CHAKRABARTY

9:50am - 11:10am Session 5: Defect Tolerance and Error Correction

1. **DEFECT TOLERANT AND ENERGY ECONOMIZED DSP PLANE OF A 3-D HETEROGENEOUS SOC**
   VIJAY K JAIN, Glenn CHAPMAN
2. **FUSE AREA REDUCTION BASED ON QUANTITATIVE YIELD ANALYSIS AND EFFECTIVE CHIP COST**
   AKHIL GARG, Prashant DUBEY
3. **LOW-DENSITY TRIPLE-ERASURE CORRECTING CODES FOR DEPENDABLE DISTRIBUTED STORAGE SYSTEMS**
   HARUHIKO KANEKO, Eiji FUJIWARA, Hiroyuki OHDE
4. **MODIFIED TRIPLE MODULAR REDUNDANCY STRUCTURE BASED ON ASYNCHRONOUS CIRCUIT TECHNIQUE**
   GONG RUI, CHEN WEI, LIU FANG, DAI KUI, WANG ZHIYING

11:30am - 12:30pm Session 6: BIST and Pseudo-Functional Test

1. **LOW POWER SOC MEMORY BIST**
   Yuejian WU, Andre IVANOV
2. **SYNTHESIS OF EFFICIENT LINEAR TEST PATTERN GENERATORS**
   AVIJIT DUTTA, Nur TOUBA
3. **AN APPROACH TO MINIMIZING FUNCTIONAL CONSTRAINTS**
   Abhijit JAS, Yi-Shing CHANG, Sreejit CHAKRAVARTY

12:30pm - 1:40pm Lunch

1:40pm - 3pm Session 7: Reliability Evaluation and Analysis

1. **RELIABILITY EVALUATION OF REPAIRABLE/RECONFIGURABLE FPGAS**
   Marco Ottavi, Salvatore Pontarelli, Vamsi Vankamamidi, Adelio Salsano, Fabrizio Lombardi
2. **RELIABILITY ANALYSIS OF SELF-REPAIRABLE MEMS ACCELEROMETER**
   Xingguo XIONG, Yu-Liang WU, Wen Ben JONE
3. **TIMING FAILURE ANALYSIS OF COMMERCIAL CPUS UNDER OPERATING STRESS**
   GWAN SEUNG CHOI, Sanghoan CHANG

4. **REAL TIME FAULT INJECTION USING ENHANCED OCD - A PERFORMANCE ANALYSIS**
   ANDRE FIDALGO, Gustavo ALVES, Jose FERREIRA

3:20pm - 4:20pm Session 8: Approaches for Soft Errors

1. **COMBINED SOFTWARE AND HARDWARE TECHNIQUES FOR THE DESIGN OF RELIABLE IP PROCESSORS**
   Cristiana BOLCHINI, Antonio MIELE, Maurizio REBAUDENGO,Donatella SCIUTO, Luca STERPONE, Massimo VIOLANTE
2. **LOW-COST HARDENING OF IMAGE PROCESSING APPLICATIONS AGAINST SOFT ERRORS**
   Ilia POLIAN, Bernd BECKER, Masato NAKAZATO, Satoshi OHTAKE, Hideo FUJIWARA
3. **ONLINE HARDENING OF PROGRAMS AGAINST SEUS AND SETS**
   CARLOS LISBOA, Luigi CARRO, Matteo REORDA, Massimo VIOLANTE

4:40pm - 6:30pm Session 9: Interactive Papers

1. **EQUIVALENT IDDQ TESTS FOR SYSTEMS WITH REGULATED POWER SUPPLY**
   CHUEN-SONG CHEN, JIEN-CHUNG LO, TIAN XIA
2. **SELF TESTING SOC WITH REDUCED MEMORY REQUIREMENTS AND MINIMIZED HARDWARE OVERHEAD**
   Ondrej NOVAK, ZDENEK PLIVA
3. **BILATERAL TESTING OF NANO-SCALE FAULT-TOLERANT CIRCUITS**
   LEI FANG, Michael HSIAO
4. **A METRIC OF TOLERANCE FOR THE MANUFACTURING DEFECTS OF THRESHOLD LOGIC GATES**
   SANDEEP DECHU, Spyros TRAGOUDAS, MANOJ KUMAR GOPARAJU
5. **SOFT ERROR MASKING CIRCUIT AND LATCH USING SCHMITT TRIGGER CIRCUIT**
   YOICHI SASAKI, KAZUTERU NAMBA, Hideo ITO
6. **INFLUENCE OF RESISTIVE BRIDGING FAULT ON CROSSTALK COUPLING EFFECTS IN ON-CHIP AGGRESSOR-VICTIM INTERCONNECTS**
   KISHORE KUMAR DUGANAPALLI, AJOY KUMAR PALIT, Walter ANHEIER
7. **SET FAULT TOLERANT COMBINATIONAL CIRCUITS BASED ON MAJORITY LOGIC**
   CARLOS LISBOA, Lorenzo PETROLI, lisson MICHELS, Fernanda KASTENSMIDT, Luigi CARRO
8. **AN IMPROVED RECONFIGURATION METHOD FOR DEGRADABLE PROCESSOR ARRAYS USING GENETIC ALGORITHM**
   Yusuke FUKUSHIMA, MASARU FUKUSHI, Susumu HORIGUCHI
9. **A BUILT-IN REDUNDANCY-ANALYSIS SCHEME FOR SELF-REPAIRABLE RAMS WITH TWO-LEVEL REDUNDANCY**
   JIN-FU LI, Yu-Jen HUANG, Da-Ming CHANG

10. **DESIGN AND EVALUATION OF AN HARDWARE ON-LINE PROGRAM-FLOW CHECKER FOR EMBEDDED MICROCONTROLLERS**
    MARCO OTTAVI, SALVATORE PONTARELLI, Alessandro LEANDRI, Adelio SALSANO
11. **RECOVERY MECHANISMS FOR DUAL CORE ARCHITECTURES**
    CHRISTIAN EL SALLOUM, Andreas STEININGER, Peter TUMMELTSHAMMER, Werner HARTER
12. **A SOFTWARE-BASED ERROR DETECTION TECHNIQUE USING ENCODED SIGNATURES**
    YASSER SEDAGHAT, Seyed Ghassem MIREMADI, MAHDI FAZELI

7:30pm Banquet

Friday, October 6

8:40am - 9:40am Session 10: Diagnosis

1. **EFFECTIVE POST-BIST FAULT DIAGNOSIS FOR MULTIPLE FAULTS**
   Hiroshi TAKAHASHI, Shuhei KADOYAMA, Yoshinobu HIGAMI, Yuzo TAKAMATSU, Koji YAMAZAKI, Takashi AIKYO, Yasuo SATO
2. **FAULT DIAGNOSIS OF ANALOG CIRCUITS BASED ON ADAPTIVE TEST AND OUTPUT CHARACTERISTICS**
   Yukiya MIURA
3. **SCAN-BASED DELAY FAULT TESTS FOR DIAGNOSIS OF TRANSITION FAULTS**
   Irith POMERANZ, Sudhakar REDDY
4. **ENHANCING DIAGNOSIS RESOLUTION FOR DELAY FAULTS BY PATH EXTENSION METHOD**
   YING-YEN CHEN, Jing-Jia LIOU

10:00am - 11:00am Session 11: Defect and Fault Tolerance in Sensors and NOCs

1. **ON-LINE MAPPING OF IN-FIELD DEFECTS IN IMAGE SENSOR ARRAYS**
   Jozsef DUDAS, Cory JUNG, Linda WU, Glenn CHAPMAN, ISRAEL KOREN, Zahava KOREN
2. **FAULT TOLERANT ACTIVE PIXEL SENSORS IN 0.18 AND 0.35 MICRON TECHNOLOGIES**
   Glenn CHAPMAN, Michelle LA HAYE, Cory JUNG, David CHEN, Jozsef DUDAS
3. **NOC INTERCONNECT YIELD IMPROVEMENT USING CROSSPOINT REDUNDANCY**
   CRISTIAN GRECU, Partha PANDE, Andre IVANOV, Res SALEH
4. **DESIGN OF LOW POWER & RELIABLE NETWORKS ON CHIP THROUGH JOINT CROSSTALK AVOIDANCE AND FORWARD ERROR CORRECTION CODING**
   Partha Pratim Pande, Amlan Ganguly, Brett Feero, Benjamin Belzer, Cristian Grecu

11:20am - 12:05pm Session 12: Test Techniques

1. **THERMAL-AWARE SOC TEST SCHEDULING WITH TEST SET PARTITIONING AND INTERLEAVING**
   Zhiyuan HE, Zebo PENG, Petru ELES, PAUL M ROSINGER, Bashir AL-HASHIMI
2. **LOAD BOARD DESIGNS USING COMPOUND DOT TECHNIQUE AND PHASE DETECTOR FOR HIERARCHICAL ATE CALIBRATIONS**
   Yong-Bin KIM, Fengming ZHANG, Warren NECOECHEA, Peter REITER, Fabrizio LOMBARDI
3. **MULTI-SITE AND MULTI-PROBE SUBSTRATE TESTING ON AN ATE**
   XIAOJUN MA, Fabrizio LOMBARDI

12:05pm - 1:15pm Lunch

1:15pm - 2:15pm Session 13: Processor Checking and Jitter

1. **OFF-CHIP CONTROL FLOW CHECKING OF ON-CHIP PROCESSOR-CACHE INSTRUCTION STREAM**
   SHANTANU DUTT, Federico ROTA, Sahithi KRISHNA
2. **THE FILTER CHECKER: AN ACTIVE VERIFICATION MANAGEMENT APPROACH**
   JOONHYUK YOO, MANOJ FRANKLIN
3. **EFFECT OF PROCESS VARIATION ON THE PERFORMANCE OF PHASE FREQUENCY DETECTOR**
   NANDAKUMAR VENUGOPAL, Nihal SHASTRY, Shambhu UPADHYAYA
4. **DATA DEPENDENT JITTER CHARACTERIZATION BASED ON FOURIER ANALYSIS**
   Tian XIA, Mu DI, Hao ZHENG

2:30pm - 3:30pm Session 14: Fault Tolerant Designs

1. **A 3-PORT REGISTER FILE DESIGN FOR IMPROVED FAULT TOLERANCE ON RESISTIVE DEFECTS IN CORE-CELL**
   LUSHAN LIU, R SRIDHAR, Shambhu UPADHYAYA
2. **A MULTIPLE-WEIGHT-AND-NEURON-FAULT TOLERANT DIGITAL MULTILAYER NEURAL NETWORK**
   TADAYOSHI HORITA, TAKUROU MURATA, ITSUO TAKANAMI
3. **VLSI IMPLEMENTATION OF A FAULT-TOLERANT DISTRIBUTED CLOCK GENERATION**
   GOTTFRIED FUCHS, Markus FERRINGER, Andreas STEININGER, Gerald KEMPF
4. **PARITY-BASED FAULT DETECTION ARCHITECTURE OF S-BOX FOR ADVANCED ENCRYPTION STANDARD**
   Arash REYHANI-MASOLEH, MEHRAN MOZAFFARI KERMANI

3:30pm Closing Remarks